Time Signal Distribution in Communication Networks Based on Synchronous Digital Hierarchy

Atsushi Imaoka and Masami Kihara
NTT Transmission Systems Laboratories
1-2356 Take, Yokosuka, Kanagawa 238-03, Japan

Abstract

A new method that uses round-trip paths to accurately measure transmission delay for time synchronization is proposed. The performance of the method in Synchronous Digital Hierarchy networks is discussed. The feature of this method is that it separately measures the initial round-trip path delay and the variations in round-trip path delay. The delay generated in SDH equipment is determined by measuring the initial round-trip path delay. In an experiment with actual SDH equipment, the error of initial delay measurement was suppressed to 30ns.

1. INTRODUCTION

Timing (frequency) signals are currently distributed in digital telecommunication networks as the reference clocks needed by digital switching and multiplexing equipment. The phase stability of the reference clocks must be better than 10µs [1]. The existing NTT (Nippon Telegraph and Telephone corporation) network has over 2000 offices that must receive timing signals. As the number of synchronous offices increases, precise timing signal distribution (phase or time distribution) without excessive delay variation is demanded for ensuring reference clock phase stability. Accurate time signal distribution is also useful for many applications such as time management in network operation systems and time stamping in distributed computer networks [2].

The Synchronous Digital Hierarchy (SDH) has been standardized by the International Telegraph and Telephone Consultative Committee (CCITT) [3] and is the basis of many existing communication networks. Timing signals for frequency synchronization are conventionally carried by 1.544Mbit/s or 6.312Mbit/s signals which are multiplexed into the digital traffic signals. In SDH systems, the frequencies derived from SDH line signals, such as 155Mbit/s, 622Mbit/s and 2.488Gbit/s, are currently being used as the reference signals for frequency synchronization.

This paper reports a time distribution method that uses the Virtual Container (VC) signals multiplexed into the SDH line signals, as the time reference signals. Time synchronous networks can be constructed flexibly to cover a wide area if VC signals are used to replace SDH line signals as the time reference signals. The delay imposed on VC signals by SDH equipment, however, varies much more widely than the waiting time jitter [4] generated in asynchronous digital networks. Precise time synchronization is only possible if the equipment delay and its variation can be accurately measured. A new method to measure VC signal transmission delay accurately is proposed in this paper. The performance of the proposed method is presented together with experimental results.

Report Documentation Page	*Form Approved* *OMB No. 0704-0188*

1. REPORT DATE **DEC 1992**	2. REPORT TYPE	3. DATES COVERED **00-00-1992 to 00-00-1992**
4. TITLE AND SUBTITLE **Time Signal Distribution in Communication Networks Based on Synchronous Digital Hierarchy**		5a. CONTRACT NUMBER
		5b. GRANT NUMBER
		5c. PROGRAM ELEMENT NUMBER
6. AUTHOR(S)		5d. PROJECT NUMBER
		5e. TASK NUMBER
		5f. WORK UNIT NUMBER
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) **NTP Transmission Systems Laboratories,1-2356 Take, Yokosuka,Kanagawa 238-03,J apan,**		8. PERFORMING ORGANIZATION REPORT NUMBER
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)		10. SPONSOR/MONITOR'S ACRONYM(S)
		11. SPONSOR/MONITOR'S REPORT NUMBER(S)

12. DISTRIBUTION/AVAILABILITY STATEMENT
 Approved for public release; distribution unlimited

13. SUPPLEMENTARY NOTES
 See also ADA267301. 24th Annual Precise Time and Time Interval (PTTI) Applications and Planning Meeting, McLean, VA, 1-3 Dec 1992

14. ABSTRACT
 see report

15. SUBJECT TERMS

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT **unclassified**	b. ABSTRACT **unclassified**	c. THIS PAGE **unclassified**	**Same as Report (SAR)**	**9**	

MUX : Multiplexing equipment   CLOCK : Reference clock equipment
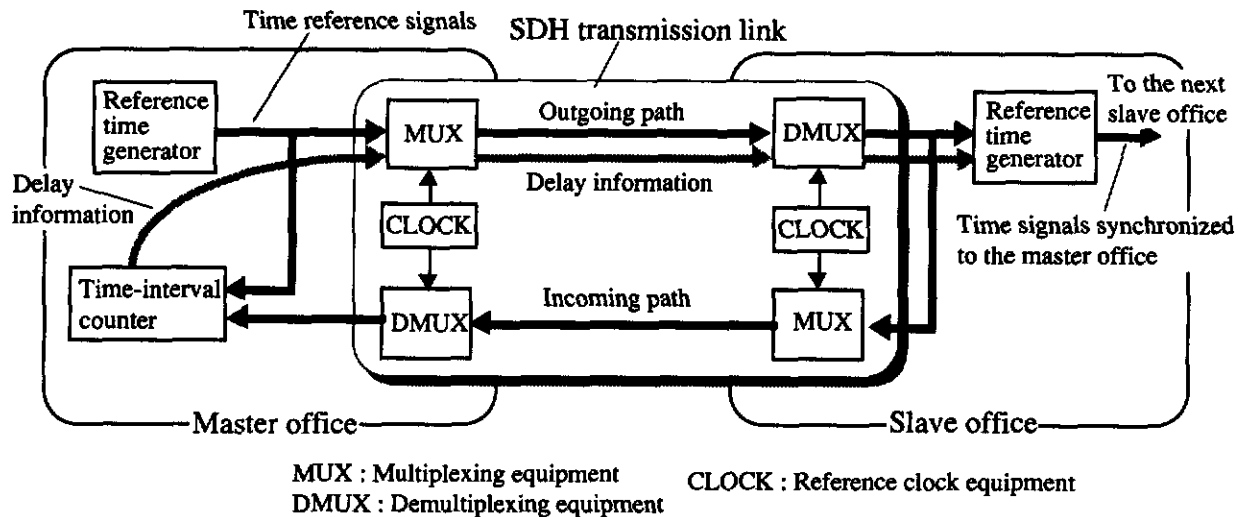DMUX : Demultiplexing equipment

Fig. 1　Basic principle of time synchronization in SDH networks.

2. TIME SYNCHRONIZATION IN SDH NETWORKS

2.1 Basic principle of time synchronization

Figure 1 shows the basic principle of time synchronization in SDH networks. The reference time generator in a slave office is synchronized to the original time generator in the master office. The master and slave offices are connected by an SDH digital terrestrial transmission link. The outgoing path delay is estimated to be one half of the round-trip path delay as measured by the master office. The round trip delay is measured continuously and the current delay information is sent to the slave office. The time signals output by the slave office are advanced by the received delay information. Time synchronization radiates outwards from the master office to all slave offices. To achieve this effect, a synchronized slave office acts as a master office to its designated neighbors. Because the delay information is updated continuously, the accuracy of time synchronization is limited by the delay difference between outgoing and incoming paths in the round-trip path. This problem is discussed in section 3.

2.2 Time signal transfer in SDH networks

In SDH networks, transferred signals are multiplexed into higher bit rate line signals which are multiples of 155Mbit/s, such as 622Mbit/s and 2.488Gbit/s. SDH line signals have a frame structure termed the Synchronous Transport Module (STM) which repeats every 125μs as shown in Fig. 2. The STM frame is a structure of 9 rows by 270 byte columns in the case of 155Mbit/s STM signals. Each STM frame consists of an information payload and overhead. The information payload includes the data signals being transferred. The overhead includes block framing information and information for maintenance, monitoring, and other operational functions. Transferred signals are structured as Virtual Containers (VCs) which also repeat every 125μs. VC signals are carried only within the STM information payload and are not carried in the overhead. The pointer included in the overhead locates the start of the VC signal within each STM frame. Because they employ pointers, STM signals can flexibly carry either synchronous or asynchronous signals.
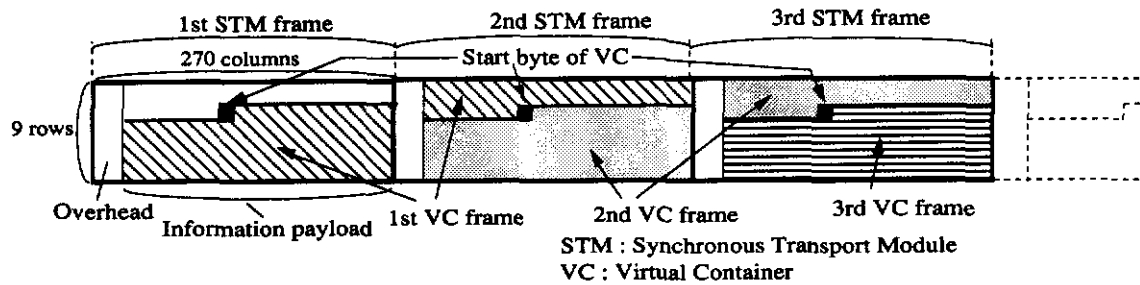
Fig. 2   Frame structure of SDH signals. Each frame has a 125μs period. The start byte of VC is indicated by the pointer included in the overhead. The phase of the VC frame is independent of the STM frame phase.

In each office, the reference clock synchronizes the SDH node, such as multiplexing and demultiplexing equipment. Reference clock in this paper means reference timing (frequency). The SDH equipment must be accurately synchronized to handle STM signals. The STM signals are synchronized to the reference clock. When an STM signal is received by an SDH node, the phase of the STM signal is terminated. The phase is not passed through the SDH equipment but is regenerated by the equipment.

VC signals "float" within the STM information payload. "Float" means that the start of the VC signal is independent of the STM frame phase as shown in Fig. 2. Because the start of the VC signal does not correspond to the start of STM information payload, the VC signal extends over two STM payloads. When a VC signal embedded in an STM signal passes through a node, the phase of the VC signal is also passed through. Thus, VC signals are more suitable to carry time reference signals than STM signals. Time synchronous networks using VC signals as time reference signals can be constructed flexibly over a wide area. This paper reports a time distribution method that uses the VC signals as time reference signals.

3. ERROR FACTORS IN DELAY MEASUREMENT

3.1 Asymmetry of transmission lines

The accuracy of measuring the round-trip delay is limited by the delay difference between outgoing and incoming paths. This delay difference is caused by delay dispersion in the SDH equipment, asymmetry of transmission line length, and the difference in delay variation of the transmission lines. We assume that two optical fibers within the same transmission cable are used as outgoing and incoming lines. Fibers included in a single cable have the same length and are set in the same environment. Thus, differences in transmission line length and delay variations are small.

Asymmetry of line length depends on the number of fiber fusion splices, in-line connectors, and equipment connections. The typical delay difference is reported to be 100ns between two SDH nodes [5]. The delay of a transmission line mainly varies with temperature. The delay variation characteristics of two fibers are very similar if they are part of the same cable. For an installed optical fiber cable 2000 km in length, the difference in delay variation between outgoing and incoming lines is reported to be below 10ns [6].

3.2 Delay dispersion in the SDH equipment

When an STM signal that is carrying a VC signal traverses an SDH node, the VC signal is embedded in a new STM signal and a new pointer must be generated to indicate the start of the VC signal. The new STM signal is synchronized to the node's reference clock. The SDH equipment delay equals the time difference between the VC signal embedded in the original STM signal and that embedded in the STM signal output from the node as shown in Fig. 3. The STM signal pointers locate the start of the VC signal to the nearest byte unit equivalent to 52Mbit/s. Hence, the use of the pointer can cause a delay difference of up to 150ns, or eight unit intervals for 52Mbit/s signals.

Figure 3 (a) and (b) show how the equipment delay of a VC signal can vary widely. When the data signals in the original payload are embedded in a payload of the new STM frame, the data in region A is little delayed, as shown in Fig. 3. The data in region B, however, is delayed by about 3 to 4 bytes (52Mbit/s) because the overhead cannot carry the data signals. Figure 3 (a) shows the delay of the VC signal when the start of the VC signal is located in region A. In this case, VC signals are delayed no more than one byte (52Mbit/s). Figure 3 (b) shows the case when the start of the VC signal is located in region B. In the case of Fig. 3 (b), the VC signal is delayed by about 3 to 4 bytes. The source of this equipment delay is the signal buffer for pointer operation. The buffer capacity is about 8 bytes (52Mbit/s), hence the maximum delay variance is about 1.2µs per node. It is necessary to measure this equipment delay accurately if we are to use VC signals as time reference signals.
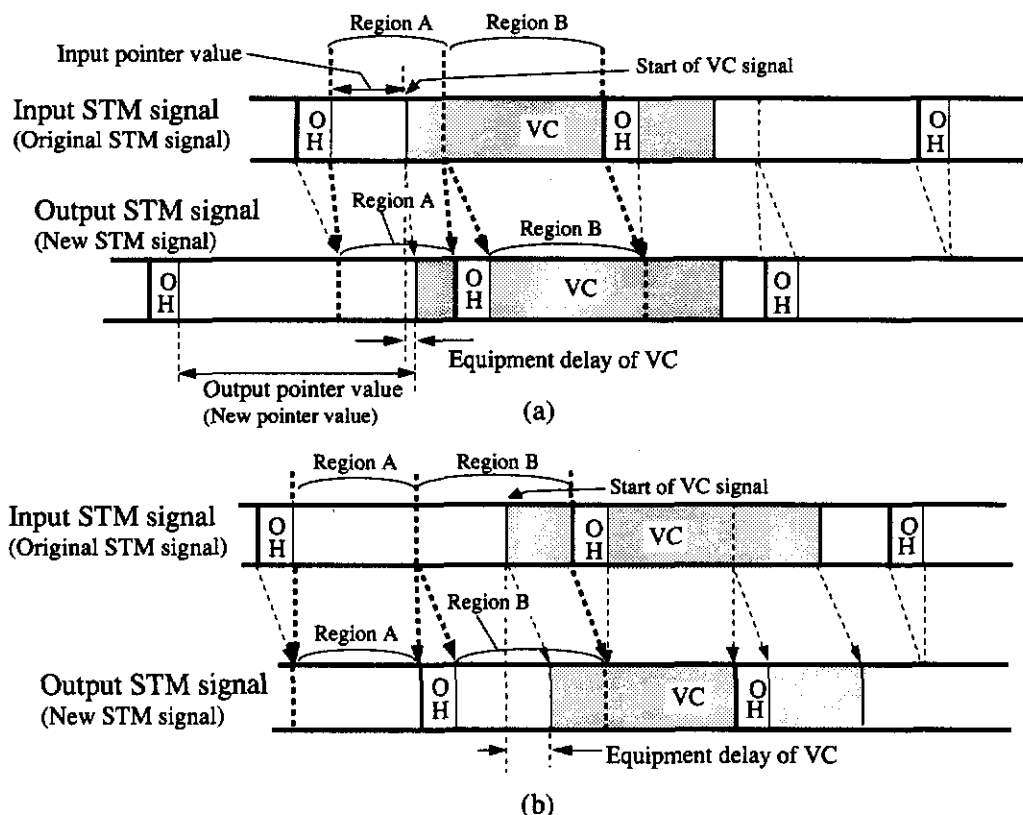

Fig. 3   **Equipment delay of VC signals. Output STM signals are synchronized to the node's reference clock.**

4. ACCURATE DELAY MEASUREMENT METHOD

4.1 Basic configuration

This section proposes an accurate delay measurement method using round-trip paths. Figure 4 shows the basic configuration of the proposed method. We consider here the measurement of the transmission delay between office A and office B. The feature of this method is that it measures the initial round-trip path delay and the round-trip path delay variations separately. In this method, VC signals embedded in STM signals are used to carry the reference time signals and to measure the initial round-trip path delay. The clock signals derived from STM line signals are used to measure the delay variations. The delay variations are measured after determining the initial delay. We assume that the reference clock in office B is usually synchronized to the frequency derived from the line signals output by office A in Fig. 4

4.2 Initial delay measurement

Before measuring the initial round-trip delay, three operations are performed to determine multiplexing and demultiplexing equipment delay accurately. Each step controls the phase difference between input signals to the equipment and the reference clock of the equipment. The phase of the input signal is delayed to minimize the equipment delay by ensuring that the signal buffer for pointer operation is empty. After determining the equipment delay, the phase of the input signal is fixed to the reference clock phase.

In the first step, B's reference clock is controlled to equalize the demultiplexing delays of office A and B. In this operation, the phase of B's reference clock is continuously advanced at a constant rate. Then, the B's reference clock is fixed when the demultiplexing delays of office A and B are equalized. The second step is to delay the phase of the reference clock of the signal generator at a constant rate. After a short time, the signal buffer for pointer operation of A's multiplexing equipment is emptied. The reference clock is then fixed when
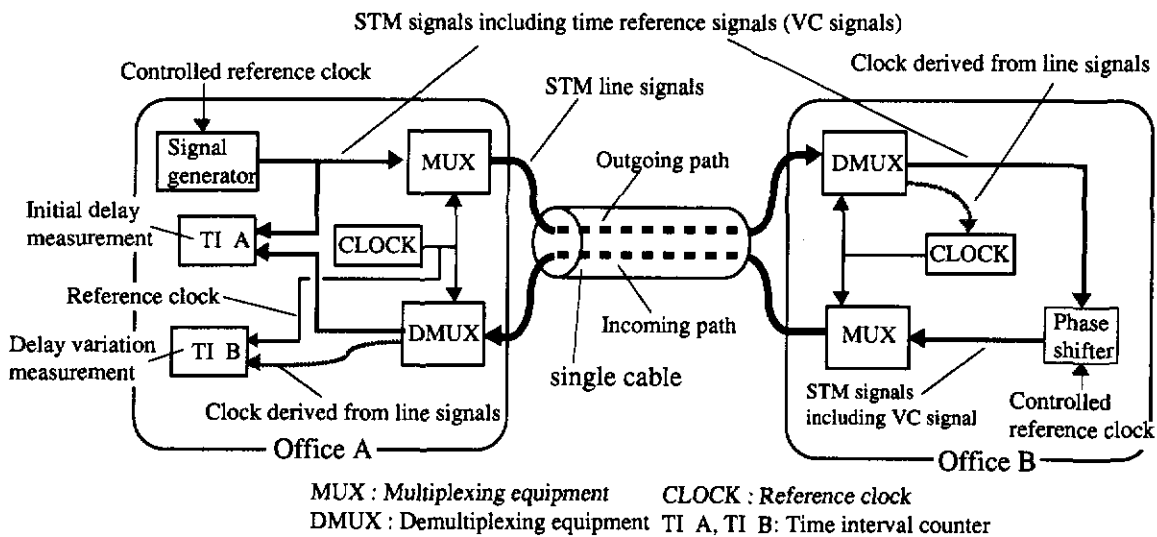

Fig. 4 Basic configuration of the proposed method.

307

the delay of A's multiplexing equipment is minimized. In the third step, the phase of the time reference signals received by the multiplexing equipment in office B is controlled by the phase shifter to minimize the delay of the multiplexing equipment in office B.

These steps are performed in such a short time that we can assume that the phase difference between the reference clocks in office A and B is stable. After the three phase control steps, the initial round-trip delay can be accurately measured. Accuracy of this measurement is confirmed in section 5 with experimental results.

4.3 Delay variation measurement

Delay variations of the round-trip path are measured by comparing the phase of the reference clock in office A and the frequency derived from incoming STM line signals. The reference clock in office B is synchronized to the frequency derived from the STM line signals received from office A. The STM signals output by office B are synchronized to B's reference clock. Hence the phase variations of the STM line signals received by office A from B, as measured in office A, equal the sum of outgoing path delay variations and incoming path delay variations. If the outgoing path delay variations are assumed to be one half of the variations measured by office A, the precision of this measurement is limited by the difference between outgoing delay variations and incoming delay variations. The precision can be below 10ns if the outgoing and incoming lines are part of the same cable [6].

The equipment delay mentioned in section 3.2 depends on the phase difference between the received STM frame and the node's reference clock. When the frame phase of the STM signal received by office B is changed by variations in transmission delay, the phase of B's reference clock varies with the frame phase of the received STM signal. Hence the demultiplexing equipment delay of office B does not change when the delay of the transmission line changes. Therefore, transmission delay and delay variations can be accurately determined by measuring round-trip delay variations after measuring the initial delay.

5. EXPERIMENT OF THE INITIAL DELAY MEASUREMENT

5.1 Setup

The initial delay measurements mentioned in section 4.2 were performed in a laboratory using the setup shown in Fig. 5. Two 622Mbit/s SDH line terminals including multiplexing and demultiplexing devices and two 20km optical fibers were used to connect the SDH terminals. One pulse per second (1pps) signals were used as the time reference signals and they were carried in 50.112Mbit/s Virtual Containers (VC-3) embedded in 155.52Mbit/s STM signals (STM-1). The STM-1 signals were multiplexed into 622Mbit/s STM line signals (STM-4) by each SDH terminal. The four reference clocks of the two SDH terminals, one for the time signal generator and one for the phase shifter, were separately controlled by four synthesizers. The phase differences of the time reference signals were measured by time-interval counters. One half of the round-trip path delay was captured by counter A while the true outgoing path delay was recorded by counter B.

5.2 Results

Figure 6 is a plot of the difference between one half of the round-trip path delay and the true outgoing path delay. The effects of the three phase control steps are shown in Fig. 6. The delay measurement error before the three steps indicates the difference in equipment delay
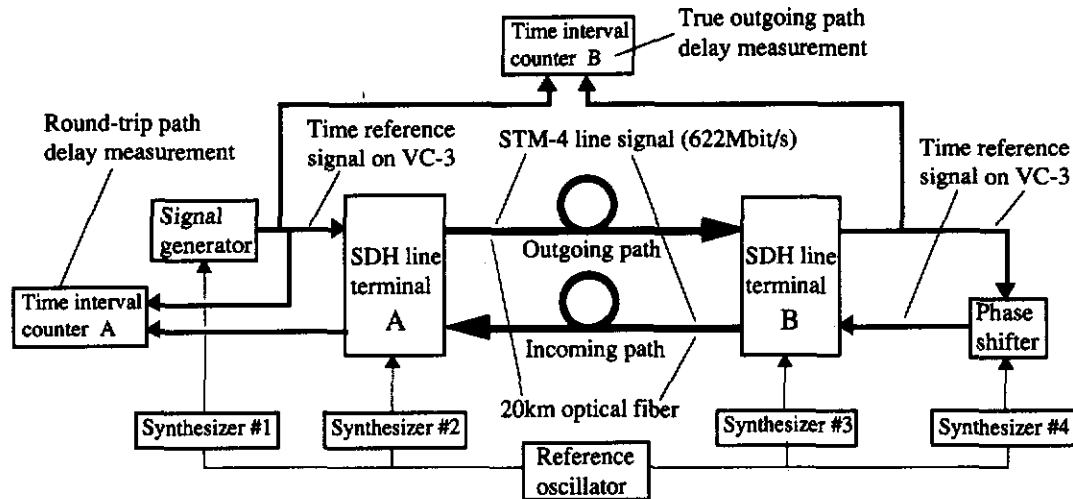

Fig. 5 Experiment setup of the initial round-trip measurement. In the first step, the phase of SDH terminal B is controlled by synthesizer #3.
In the second step, the phase of input time signals to SDH terminal A from the signal generator is controlled by synthesizer #1.
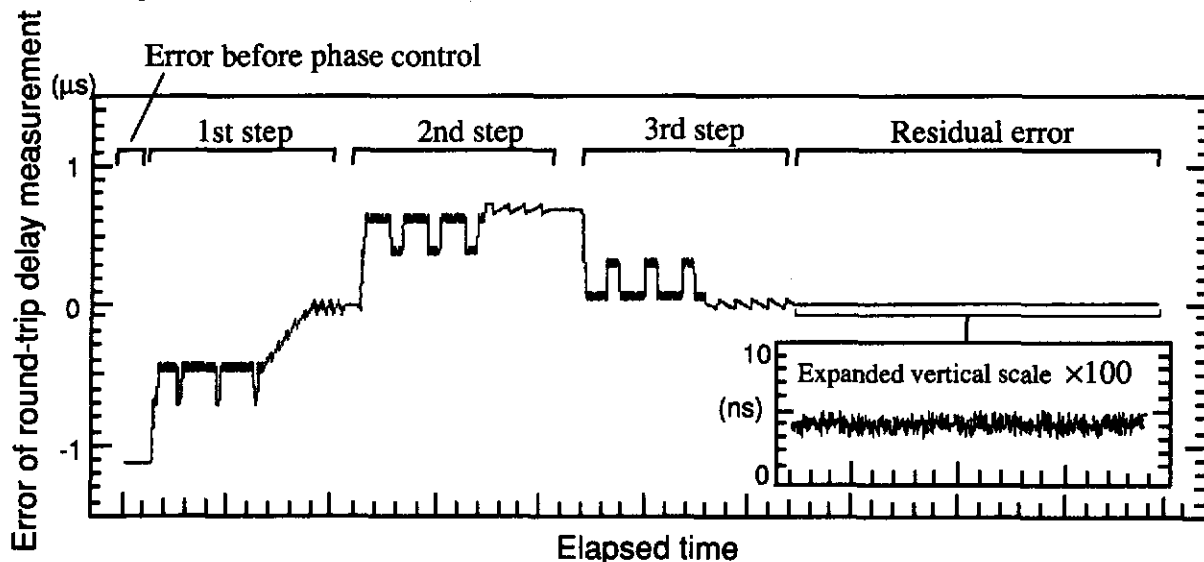The phase of input time signals to SDH terminal B is controlled by synthesizer #4 in the third step.

Fig. 6 The effect of the three phase control steps and the error of the round-trip delay measurement. The error before phase control was about -1.2μs and the residual error after the phase control was 5ns in this experiment.
The error before the control varied in the range from -1.2μs to +1.2μs as determined by repeated experiments. The residual error after control varied only 30ns in repeated experiments.

309

of the outgoing and incoming paths. The absolute value of maximum error before the three steps was 1.2μs as determined by repeated experiments. The residual error of the initial delay measurement after the three steps lay within the range of -15ns to +15ns in repeated experiments. The residual error is probably caused by phase control error and delay variations below the unit interval of the 50Mbit/s VC signals in the two SDH terminals.

Because actual measurements will be made on actual transmission paths, asymmetric path lengths will cause a residual error in initial delay measurement. Typical delay asymmetry is reported to be 100ns [5],[6], hence it will be the dominant source of initial delay measurement error.

6. CONCLUSION

An accurate delay measurement method that uses round-trip paths for time signal distribution in SDH networks was proposed. The feature of this method is that it measures the initial round-trip path delay and round-trip path delay variations separately. In an experiment using actual SDH equipment, the fluctuation of the equipment delay was suppressed to 30ns with a new three step process. This residual fluctuation is smaller than the typical delay asymmetry, which is reported to be 100ns, of actual paired transmission lines that will be used to effect the round-trip paths. The accuracy of absolute time synchronization is limited by the residual fluctuation of equipment delay and the delay asymmetry of the paired lines. On the other hand, the precision of delay variation measurement can be below 10ns. Hence the instability of time synchronization will be within 10ns.

REFERENCE

[1] CCITT Recommendation G.824, Blue Book, Oct. 1988.

[2] W. D. Grover and T. E. Moore, "Precision Time-Transfer in Transport Networks Using Digital Cross-Connect Systems," IEEE Trans. Communications, vol. 38, pp.1325-1332, Sep. 1990.

[3] CCITT Recommendation G.707, G.708, G.709, Blue Book, 1989.

[4] R. D. Hall and M. J. Snaith, "Jitter Specification in Digital Network," Post Office Electrical Engineers' Journal, vol. 72, pp.96-101, July 1979.

[5] M. Kihara and A. Imaoka, "Time Concurrency / Phase-Time Synchronization in Digital Communications Networks," Proc. 22nd PTTI, pp. 367-374, 1990.

[6] A. Imaoka and M. Kihara, "Long Term Propagation Delay Characteristics of Telecommunication Lines," IEEE Trans. Instrumentation and Measurement, vol. 41, Oct. 1992 (in press).

QUESTIONS AND ANSWERS

R. Brown, Bellcore: I was wondering on your jitter of one nanosecond; was that optical line jitter?

A. Imaoka: It was not line jitter. It was equipment jitter.

R. Brown: Is it payload jitter like the virtual container jitter or is it optical line jitter?

A. Imaoka: The jitter includes all those.